

REMARKS

Claims 1-20 were presented for examination in the present application and remain pending upon entry of the instant response. Claims 1 and 11 are independent.

Independent claims 1 and 11, as well as dependent claims 2-5, 9, 12-15, and 19-20, were rejected under 35 U.S.C. §102 over U.S. Patent No. 6,356,821 to Yoshida (Yoshida). Dependent claims 6-8 and 16-18 were rejected under 35 U.S.C. §103 over Yoshida in view of U.S. Publication No. 2003/0115543 to Emde et al. (Emde). Dependent claim 10 was rejected under 35 U.S.C. §103 over Yoshida in view of U.S. Patent No. 4,794,601 to Kikuchi et al. (Kikuchi).

Applicants respectfully maintain the traversal of this rejection.

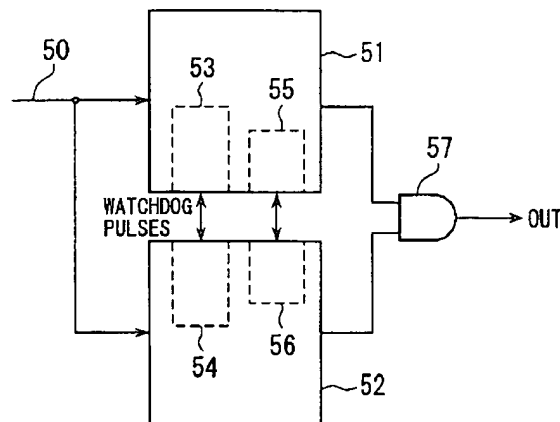
Independent claim 1 recites, in part, the step of “converting said first and at least one more process signals to a single process signal for further system-based processing to carry out logic operations on a single-signal basis for identifying the same event”. Independent claim 11 recites, in part, a converter for conversion of said plurality of process signals to a single process signal, said single process signal being capable of being transmitted via one channel to carry out logic operations on a single-signal basis to identify the same event.

The Office Action asserts that Yoshida discloses logic operations that occur on a single signal output from comparing circuit 57 in order to identify if there has been a fault. Further, the Office Action asserts that comparing circuit 57 itself may not carry out logic operations, as its main purpose is to convert two signals to one and it is this one signal upon which Yoshida executes its logic operation to detect a fault. See page 2, lines 8-14 of the Office Action dated May 14, 2007

Applicants respectfully disagree.

The extent of disclosure in Yoshida of circuit 57 begins at col. 1, line 30 and ends at line 62, and is shown in FIG. 5. For ease of analysis, FIG. 5 is reproduced below in its entirety.

FIG. 5



PRIOR ART

With respect to FIG. 5, the pertinent part of Yoshida discloses an electronic control unit that comprises a duplicate structure of a pair of microcomputers 51, 52. An input signal 50 is commonly supplied to both of the microcomputers 51 and 52, which include monitoring circuits 53, 54 and communication/ monitoring circuits 55, 56, respectively. Comparing circuit 57 **compares** operation results outputted from **both microcomputers 51 and 52**. When the operation results do not coincide, it is determined that there is any fault in operational function and the like of a processing system including the microcomputers 51 and 52, and **the comparing circuit 57 outputs a fault signal indicating that there is a fault condition in the processing system**.

Again, the Office Action asserts that Yoshida discloses “logic operations that occur on a single signal output from comparing circuit 57 in order to identify if there has been a fault”. Applicants submit that the disclosure in Yoshida simply does not support or enable such an interpretation.

Rather, Yoshida clearly discloses that comparing circuit 57 compares operation results outputted from both microcomputers 51 and 52.

Further, the Office Action asserts that “comparing circuit 57 itself may not carryout out logic operations, as it’s main purpose is to convert two signals to one, however logic operations are executed on the single signal output of comparing circuit 57”. See page 2, line 11-13 of the Office Action dated May 14, 2008. Applicants also submit that the disclosure in Yoshida simply does not support or enable such an interpretation.

Rather, Yoshida clearly discloses that comparing circuit 57 not only does the comparing, but also that the circuit 57 itself outputs the fault signal.

Thus, Applicants submit that Yoshida simply fails to disclose or suggest or enable a reading of its disclosure to disclose or suggest the method of claim 1 that converts “said first and at least one more process signals to a single process signal for further system-based processing to carry out logic operations on a single-signal basis for identifying the same event” or claim 11 that recites “a converter for conversion of said plurality of process signals to a single process signal, said single process signal being capable of being transmitted via one channel to carry out logic operations on a single-signal basis to identify the same event”.

Accordingly, Applicants respectfully maintain that the Office Action has misapplied Yoshida to claim 1. Clearly, Yoshida does not carry out logic operations on a single-signal basis to identify the same event. Rather, Yoshida compares two inputs to identify the fault condition.

Emde was merely asserted as disclosing transmission of protected signals with respect to dependent claims 6-8. However, Emde simply fails to disclose or suggest the logic operations on a single-signal basis to identify the event of claim 1 or claim 11.

Kikuchi was merely asserted as disclosing transmission signals via separate channels with respect to dependent claim 10. However, Kikuchi simply fails to disclose or suggest the logic operations on a single-signal basis to identify the event of claim 1 or claim 11.

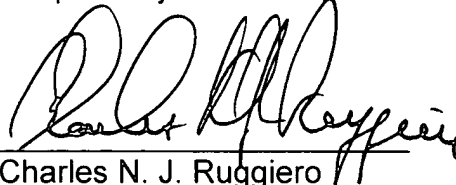
Accordingly, Applicants submit that Yoshida, alone or in combination with Emde and/or Kikuchi fails to disclose or suggest independent claims 1 and 11, or claims 2-10 and 12-20 that depend therefrom, respectively. Reconsideration and withdrawal of the rejection to claims 1-20 are respectfully requested.

In view of the above, it is respectfully submitted that the present application is in condition for allowance. Such action is solicited.

If for any reason the Examiner feels that consultation with Applicants' attorney would be helpful in the advancement of the prosecution, the Examiner is invited to call the telephone number below.

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Respectfully submitted,



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